10/692,921 PLEASE SCAN FOR THE RECORD

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Board Decision reviewed by examiner. /BH/ 8/26/08

Ex parte ERIC A. JOHNSON
and DAVID V. CALETKA

Appeal 2007-3660
Application 10/692,921[1]
Technology Center 2800

Decided: July 7, 2008

Before KENNETH W. HAIRSTON, ANITA PELLMAN GROSS, and MARC S. HOFF, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from a Final Rejection of claims 1, 2, 5-12, and 15-20.[2] We have jurisdiction under 35 U.S.C. § 6(b).

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[1] Application filed October 24, 2003. The real party in interest is International Business Machines Corporation.

We affirm-in-part.

Appellants' invention relates to a method of producing opto-electronic cards and printed circuit boards which are adapted to provide for the passive alignment of Vertical Cavity Surface Emitting Lasers (VCSELs) to waveguides (Spec. 1). Precise and passive alignment of VCSELs and receiver chips relative to an opto-electronic card (or printed circuit board) may be attained by means of a C4 solder reflow (Spec. 5). The surface tension of molten solder aligns the chips to the solder pads on the card or printed circuit board (*Id.*).

Claim 1 is exemplary:

1. An opto-electronic package facilitating the passive alignment of VCSELs to waveguides; said package comprising:

a substrate bearing a first surface;

a first cladding layer positioned on said first surface of said substrate;

a contact pad positioned on at least a position of the surface of said first cladding layer;

a second cladding layer located on a further surface position of said first cladding layer;

a waveguide channel being positioned in said second cladding layer;

optical means being in optical communication with said waveguide channel in said second cladding layer and in electrical connection with said contact pad on said first cladding layer, at least one transmitter/receiver chip being coupled to said surface of said second cladding layer; and

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[2] Claims 3, 4, 13, and 14 have been canceled. Claims 21-23 stand withdrawn from consideration.

at least one transmitter/receiver chip being coupled to said surface of said second cladding layer through the interposition of C4-joints.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Yoshizawa	US 2002/0084522 A1	Jul. 4, 2002
Towle	US 6,834,133 B1	Dec. 21, 2004
Oono	US 2005/0105860 A1	May 19, 2005 (filed February 23, 2004)

Claims 1, 8, 11, and 18 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Towle.

Claims 2, 9, 10, 12, 19, and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Towle in view of Oono.

Claims 5-7 and 15-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Towle in view of Yoshizawa.

Appellants contend, *inter alia*, that Towle does not teach at least one transmitter/receiver chip being coupled to the surface of the second cladding layer, with or without the interposition of C4 joints (Br. 5), and that the combination of Towle and Yoshizawa lacks a teaching of low expansion materials to minimize strains in C4 joints (Br. 8-9).

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Brief (filed March 20, 2006) and the Answer (mailed May 1, 2006) for their respective details.

ISSUE

There are three principal issues in the appeal before us.

The first issue is whether the Examiner erred in holding that Towle teaches a transmitter/receiver chip coupled to the surface of a cladding layer, with or without the interposition of C4 joints.

The second issue is whether the Examiner erred in holding that Towle and Oono are properly combinable to achieve the instant invention.

The third issue is whether Towle in combination with Yoshizawa teaches low expansion materials to minimize strains in C4 joints, or an index-matched adhesive coupling the second cladding layer directly to at least one transmitter/receiver chip.

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

The Invention

1. According to Appellants, they have invented a method of producing opto-electronic cards and printed circuit boards which are adapted to provide for the passive alignment of Vertical Cavity Surface Emitting Lasers (VCSELs) to waveguides (Spec. 1).

2. Precise and passive alignment of VCSELs and receiver chips relative to an opto-electronic card (or printed circuit board) may be attained by means of a C4 solder reflow (Spec. 5). Thus, it is well known in the art that the surface tension of molten solder aligns the chips to the solder pads on the card or printed circuit board (*Id.*).

Towle

3. Towle teaches methods to simultaneously optically and electrically couple an optoelectronic chip to a waveguide and substrate (col. 1, ll. 9-11).

4. Towle teaches a waveguide (112) and a transmitter/receiver (optoelectronic chip 114, having optically active area 116) coupled to the surface of the waveguide (Figs. 1, 2; col. 3, l. 56 – col. 4, l. 16).

5. Towle teaches that its transmitter/receiver chip is "flip-chip bonded" to the waveguide and contact pad (col. 3, l. 56 – col. 5, l. 9).

6. "During the bonding process, melting and hardening the solder bumps 126, 128 tends to draw the flip-chip 114 and the substrate 110 together in alignment due to a surface tension of the molten solder bumps 126 and 128" (col. 4, ll. 47-50).

Oono

7. Oono teaches an optoelectronic device that couples a VCSEL to an optical waveguide, including the use of organic materials in claddings (para. [0171]).

Yoshizawa

8. Yoshizawa teaches an optoelectronic package where the substrate is formed of a material having a low thermal expansion coefficient such as a glass-fiber epoxy resin that reduces the stress of the flip chip bond by reducing the difference between the coefficients of thermal expansion of the substrate and the chip (para. [0021]).

PRINCIPLES OF LAW

Anticipation is established when a single prior art reference discloses expressly or under the principles of inherency each and every limitation of the claimed invention. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1347 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79 (Fed. Cir. 1994).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734, (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, (1966). *See also KSR*, 127 S. Ct. at 1734 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.")

ANALYSIS

Claims 1 and 8

We select claim 1 as representative of this group, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

Appellants argue that Towle does not teach at least one transmitter/receiver chip being coupled to the surface of the second cladding layer, nor that said at least one transmitter/receiver chip is coupled to the surface of the second cladding layer through the interposition of C-4 joints (Br. 5). We are not persuaded that Towle fails to teach these features.

Towle teaches a waveguide (112) and a transmitter/receiver (optoelectronic chip 114, having optically active area 116) coupled to the surface of the waveguide (FF 4). The Examiner asserts that waveguide 112 "includes a core and cladding, since all waveguides include a core section surrounded by a cladding section so as to confine light within the core" (Ans. 5). We consider that statement to be equivalent to an assertion that the cladding layer around the waveguide is considered to be inherently present in Towle. Appellants present no rebuttal to the Examiner's position, and we have no reason to find it to be erroneous.

With regard to the interposition of C4 joints, Towle teaches that its transmitter/receiver chip is "flip-chip bonded" to the waveguide and contact pad (FF 5). The Examiner asserts that flip chip bonding is conventional and involves the use of C4 joints (Ans. 3, 6). The Examiner took the same position in the Final Rejection, and Appellants have not contested the Examiner's position regarding the use of C4 joints in flip chip bonding. The Examiner further notes that Towle's description of the flip chip bonding process matches Appellants' discussion of C4 joints. Appellants explain that:

> Precise and passive alignment of VCSELs and receiver chips relative to the opto-electronic card (or printed circuit board) may be attained by means of a C4 solder reflow. Thus, it is well known in the

> art that the *surface tension of molten solder aligns the chips to the solder pads on the card or printed circuit board*.
> FF 2 (emphasis added).

Towle teaches that "[d]uring the bonding process, melting and hardening the solder bumps 126, 128 tends to draw the flip-chip 114 and the substrate 110 together in alignment *due to a surface tension of the molten solder bumps 126 and 128*" (FF 6) (emphasis added). Taking the Examiner's assertion that flip chip bonding includes the use of C4 joints together with the identity of function between Appellants' invention and Towle, we agree with the Examiner that Towle teaches at least one transmitter/receiver chip being coupled to the surface of the second cladding layer through the interposition of C4 joints, as claim 1 requires.

Because we find that Towle teaches all of the limitations of claim 1, we do not find error in the Examiner's rejection of claim 1, nor of claim 8 not separately argued, under 35 U.S.C. § 102(e).

Claims 11 and 18

Appellants rely on the same arguments for patentability of claims 11 and 18 that were made with respect to claims 1 and 8. Because we affirm the rejection of claims 1 and 8 *supra*, we therefore also affirm the rejection of claims 11 and 18, for the same reasons.

Claims 2, 9, 10, 12, 19, and 20

These claims stand rejected as obvious over Towle in view of Oono. The filing date of the application under appeal is October 24, 2003. Oono's publication date of May 19, 2005 does not qualify it as prior art. Oono's filing date, February 23, 2004, is also later than Appellant's filing date. Therefore, the Oono reference does not qualify as prior art.

Because no proper rejection over Towle in view of Oono has been established, we find error in the Examiner's rejection of claims 2, 9, 10, 12, 19, and 20 as obvious over Towle in view of Oono.

Claims 5-7 and 15-17

Appellants argue that Towle in combination with Yoshizawa fails to disclose or suggest low expansion materials to minimize strains in C4 joints, or index-matched adhesive, as recited in the claims at issue (Br. 8-9).

We are not persuaded by Appellants' arguments. We agree with the Examiner that Yoshizawa teaches an optoelectronic package where the substrate is formed of a material having a low thermal expansion coefficient such as a glass-fiber epoxy resin that reduces the stress of the flip chip bond by reducing the difference between the coefficients of thermal expansion of the substrate and the chip (FF 8). Because we find *supra* that the joints of conventional flip chip bonded chips (such as used in Towle) are C4 joints, the combination of Towle and Yoshizawa teaches minimizing strain on C4 joints.

Therefore, we do not find error in the Examiner's rejection of claims 5-7 and 15-17 as obvious over Towle in view of Yoshizawa.

CONCLUSION OF LAW

We conclude that Appellants have not shown that the Examiner erred in rejecting claims 1, 5-8, 11, and 15-18. Claims 1, 5-8, 11, and 15-18 are not patentable over the applied prior art references. We conclude that the

Examiner erred in rejecting claims 2, 9, 10, 12, 19, and 20. On the record before us, claims 2, 9, 10, 12, 19, and 20 have not been shown to be unpatentable.

DECISION

The Examiner's rejections of claims 1, 5-8, 11, and 15-18 are affirmed. The Examiner`s rejection of claims 2, 9, 10, 12, 19, and 20 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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